## AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method, comprising:

providing a semiconductor substrate;

forming electrically conductive columns [[on]] over the semiconductor substrate;

forming electrically conductive rows crossing [[over]] the electrically conductive columns;

forming a plurality of memory components each having a resistance value corresponding to multiple logical bits; and

forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column, wherein the non-volatile memory cells are formed without transistors for reduced space usage on the semiconductor substrate by each memory cell.

2. (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:

providing a semiconductor substrate;

forming electrically conductive columns over the semiconductor substrate;

forming electrically conductive rows crossing the electrically conductive columns;

forming a plurality of memory components each having a resistance value corresponding to multiple logical bits; and

forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column,

wherein [[each]] the memory ~~component is~~ components are formed to have [[a]] varying resistance ~~value~~ values based on ~~a thickness~~ at least one of: (1) varying thicknesses of electrically resistive ~~material~~ materials that ~~forms an individual~~ are part of respective memory ~~component~~ components; (2) varying areas of electrically resistive materials that are part of respective memory components; and (3) varying geometric shapes of electrically resistive materials that are part of respective memory components.

3. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on an area of electrically resistive material that forms an individual memory component.

4. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on a geometric shape of electrically resistive material that forms an individual memory component.

5. (Original) A method as recited in claim 1, wherein the plurality of memory components are each formed to have a different resistance value based on a different area of electrically resistive material that forms a memory component.

6. (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:

providing a semiconductor substrate;

forming electrically conductive columns over the semiconductor substrate;

forming electrically conductive rows crossing the electrically conductive columns;

forming a plurality of memory components each having a resistance value corresponding to multiple logical bits; and

forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column,

wherein the plurality of memory components are each formed to have a resistance value based on a rectangular geometric shape of electrically resistive material that forms a memory component, at least some of the rectangular geometric shapes having different resistance values corresponding to an area of a rectangular geometric shape.

7. (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:

providing a semiconductor substrate;

forming electrically conductive columns over the semiconductor substrate;

forming electrically conductive rows crossing the electrically conductive columns;

forming a plurality of memory components each having a resistance value corresponding to multiple logical bits; and

forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column,

wherein forming the non-volatile memory cells comprises:

forming a first memory cell having a memory component that indicates logical bits 00 (zero-zero);

forming a second memory cell having a memory component that indicates logical bits 01 (zero-one);

forming a third memory cell having a memory component that indicates logical bits 10 (one-zero); and

forming a fourth memory cell having a memory component that indicates logical bits 11 (one-one).

8. (Currently Amended) ~~A method as recited in claim 1,~~ A method, comprising:

providing a semiconductor substrate;

forming electrically conductive columns over the semiconductor substrate;

forming electrically conductive rows crossing the electrically conductive columns;

forming a plurality of memory components each having a resistance value corresponding to multiple logical bits; and

forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column,

wherein forming the non-volatile memory cells comprises:

forming a first memory cell that indicates logical bits 00 (zero-zero) corresponding to a first resistance value based on an area of electrically resistive material that forms a memory component in the first memory cell;

forming a second memory cell that indicates logical bits 01 (zero-one) corresponding to a second resistance value based on an area of electrically resistive material that forms a memory component in the second memory cell;

forming a third memory cell that indicates logical bits 10 (one-zero) corresponding to a third resistance value based on an area of electrically resistive material that forms a memory component in the third memory cell; and

forming a fourth memory cell that indicates logical bits 11 (one-one) corresponding to a fourth resistance value based on an area of electrically resistive material that forms a memory component in the fourth memory cell.

9. (Original) A method as recited in claim 1, wherein forming the plurality of memory components comprises forming individual memory components with a resistor in series with a diode.

10. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing the memory component to light.

11. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing electrically resistive material forming the memory component to light.

12. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing the memory component to heat.

13. (Original) A method as recited in claim 1, further comprising configuring the resistance value of an individual memory component by exposing electrically resistive material forming the memory component to heat.

14. (Currently Amended) A method as recited in claim 1, wherein forming the non-volatile memory cells comprises:

forming a first non-volatile memory cell by connecting a first memory component between an electrically conductive row and a first electrically conductive column, the first non-volatile memory cell formed as part of a first layer of non-volatile memory cells; and

forming a second non-volatile memory cell by connecting a second memory component between the electrically conductive row and a second electrically conductive column, the second non-volatile memory cell formed as part of a second layer of non-volatile memory cells, the second layer formed over the first layer.

15. – 22. (Cancelled)

23. (New) A method comprising:

providing electrically conductive row traces and electrically conductive column traces;

providing memory cells having respective resistive components, the resistive components connected between respective row and column traces without connecting through isolation circuitry,

an individual one of the resistive components having a resistance value representing plural logical bits.

24. (New) The method of claim 23, wherein providing the memory cells having respective resistive components connected between respective row and column traces without passing through isolation circuitry comprises providing the memory cells having respective resistive components connected between respective row and column traces without passing through transistors.

25. (New) The method of claim 23, wherein providing the memory cells having respective resistive components connected between respective row and column traces without passing through isolation circuitry comprises providing the memory cells having respective resistive components connected between respective row and column traces without passing through transistors or diodes.

26. (New) The method of claim 23, further comprising:

connecting a selected one of the column traces to a first voltage;

connecting a selected one of the row traces to a second voltage such that electrical current passes through a selected memory cell; and

connecting unselected column and row traces to voltages generally equal to the first voltage to reduce parasitic electrical current through unselected memory cells.

27. (New) The method of claim 26, wherein connecting the selected row trace to the second voltage comprises connecting the selected row trace to ground.

28. (New) The method of claim 23, wherein providing the memory cells comprises providing the memory cells in at least a first layer and a second layer, the first layer being provided over the second layer.

29. (New) The method of claim 23, wherein providing the memory cells having respective resistive components comprises providing resistive components having varying resistance values based on at least one of: (1) varying thicknesses of electrically resistive materials that are part of respective resistive components; (2) varying areas of electrically resistive materials that are part of respective resistive components; and (3) varying geometric shapes of electrically resistive materials that are part of respective resistive components.

30. (New) The method of claim 1, wherein forming the non-volatile memory cells comprises connecting the memory components of respective memory cells between respective columns and rows without connecting through a transistor or diode.